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| **KING SAUD UNIVERSITY**  **COLLEGE OF COMPUTER AND INFORMATION SCIENCES Computer Science Department** | | |
| **CSC 227: Operating System** | **Tutorial# 1**  **Due: Sunday, February 19 (12-1)** | **2nd Semester 1437-1438**  **Spring 2017** |

**Question#1:**

*Circle ALL correct answers. Note that there might be multiple correct answers; also, there might be no correct answer.*

1. The operating system components include:
   1. Hardware.
   2. Users.
   3. **Kernel.**
   4. **System programs.**
2. Which of the following is NOT a multi-user environment computer:
   1. Minicomputer.
   2. Mainframe.
   3. Supercomputer.
   4. Workstation.
3. Which of the following is NOT true about the bootstrap program:
   1. It loads the kernel.
   2. **It is part of the kernel.**
   3. It is stored in ROM.
   4. Exists in memory as long as the computer in on.
4. The operating system deals with the printer through:
   1. Kernel.
   2. **Printer controller.**
   3. Bootstrap.
   4. **Printer driver.**
5. After a H/W interrupt, the CPU has to continue the process that has been paused. Which of the following helps the CPU to do that:
   1. **Process state.**
   2. **Process Control Block (PCB).**
   3. Interrupt controller.
   4. Interrupt request.
6. Which of the following is NOT true about the S/W interrupt:
   1. Occurs unintentionally.
   2. Causes faults.
   3. Occurs intentionally.
   4. **Asynchronous.**
7. Which is the following represents the correct order of memory in terms of speed:
   1. Register – main memory – cache memory
   2. Main memory – register – cache memory
   3. **Register – cache memory – main memory**

**Question#2:**

*Write* ***clearly*** *numbers in front of each statement to indicate the correct order of conducting an interrupt?*

*Note that there may non-applicable statements. In this case, write N/A in the second column.* ***DON’T LEAVE IT BLANK****.*

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| Action | Order |
| The CPU sends the number of the interrupt to the interrupt vector | **6** |
| The CPU sends a signal to the Operating System | **N/A** |
| The CPU resumes the execution of the user’s program | **9** |
| The CPU checks the status of the device | **N/A** |
| The CPU suspends the execution of the user’s program | **4** |
| The CPU receives a signal from the device controller | **1** |
| The CPU loads the relevant interrupt handler | **7** |
| The CPU finishes the execution of the current instruction | **3** |
| The CPU acknowledges the w of the interrupt signal | **2** |
| The CPU executes the interrupt handler | **8** |
| The CPU saves the state of the currently running program | **5** |

**Question#3:**

1. How many times addresses are found in cache, given that the total number of cache access is 2000 and the cache performance is 23.5 %  
   Performance =

23.5 =

= 470

1. A computer system is provided with two levels of caches with access times (T) of 8 and 10 ms respectively. The main memory (RAM) access time is 30 ms. Given that the miss ratios (MR) are 0.7 and 0.3 for L1 and L2 caches respectively. What is the average access time (TAVR) of the whole system?

If fount in L1 cache = L1 hit rate \* access or hit time for L1

+ If found in L2 cache = L1 miss rate \* access foe hit time for L2 (L1 miss penalty)

+ if found in RAM = L2 miss rate \* access or hit time for RAM (L2 miss penalty)

TAVR = HR L1 \* T L1 + MR L1 \* (T L1 + T L2) + MR L2 \* (T L2 + T RAM)

TAVR = 0.3 \* 8 + 0.7 \* 18 + 0.3 \* 40 = 27ms